Remarks

Claims 1-40 are pending in the application. Applicant notes with appreciation that the Examiner has indicated that Claims 1, 11, 21, 33-39 and their progeny are directed to allowable subject matter. It is also noted that Claims 1-30 and 40 are objected to, but not rejected. Claims 31 and 39 are amended as per the Examiner's recommendation.

ARGUMENT

Claims 1, 11, 21, 31 and 39 are objected to because the Examiner asserts that the drawings and specification disclose "only the control and access signals" and not a plurality of data values, as recited in the claims. This objection is respectfully traversed and Claims 1, 11, 21, 31 and 39 are believed allowable based on the following discussion.

The specification, on page 5, discloses:

> "In one embodiment, a signal tap 215 is utilized to link the FPGA 202 to the address and control signals, as well as the apparatus' 214 chip select, on the host's memory bus 206, regardless of to which device the on-board SDRAM bus switch 212 is connected, so that it can monitor the values driven by the host 208." [emphasis added]

As disclosed, the tap line may receive address and control signals, as well as, chip select values, and further monitor values driven by the host. Figure 2 clearly shows that the host 208 is coupled to the first device via the memory bus 206 and the tap line 215. The memory bus 206 is labeled with address, control and data signals. Thus, it is inherent in Figure 2 that a tap line may *communicate said plurality of data values between said signal line and said first device.* It is not necessary to all embodiments of the claimed invention that the tap line communicate more than the address and control signals, but it is certainly possible for it to do so, as the tap line is coupled with the memory bus, which sends a plurality of data values. Thus, it is clearly disclosed that the tap line may communicate a plurality of data signals. In addition, the original claims are part of the specification as originally filed. The original claims recite "a tap line to communicate said plurality of data values between said signal line and said first device." Therefore, a plurality of data values is disclosed in the specification as filed.

Further, the Examiner asserts that Claims 1, 11, 21 and 39 recite "predetermined sequence of address locations on the tap line," but that the terms "data values" and "address locations" should be consistent. The Examiner misunderstands the distinction. The tap line

PAGE 10/13 * RCVD AT 8/10/2005 6:59:02 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/0 * DNIS:2738300 * CSID:4087208381 * DURATION (mm-ss):05-02

communicates a plurality of data values, as discussed above. Address locations are just one form that the communicated data values may take. For instance, the tap line may receive control signals or chip select signals, but the event is initiated upon detection of the address locations. Thus, other values may be received by the tap line without initiating the event. The recitation of elements in Claims 1, 11, 21 and 39 is therefore consistent with the actual operation of embodiments of the claimed invention and no correction/amendment is necessary.

Claims 31 and 39 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. This rejection is moot based on the above amendments, as suggested by the Examiner.

Claims 31-32 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 5,687,346 to Shinohara (hereinafter "Shinohara"). This rejection is respectfully traversed and Claims 31-32 are believed allowable based on the foregoing and following discussion.

The Examiner has mischaracterized the teaching of Shinohara as compared to Applicant's claimed invention. Shinohara teaches a PC card having a memory bus 20 connected to the host CPU 12 via a bus switch 31 and inner card bus 11. If compared to Applicant's claimed invention, the host, as recited in Claim 31, would be the CPU 12 as taught by Shinohara. The first device, as recited in Claim 31, is a secondary computing device for computationally intensive tasks. The Examiner mischaracterizes the first device as Shinohara's CPU 12. Further, The Examiner fails to show a tap line to communicate data values between the memory bus and first device. Shinohara teaches a PC card inserted into a host computer.

However, even if one analogizes Shinohara's host computer (external to the PC card) as Applicant's host, and Shinohara's CPU to Applicant's first device, Shinohara neither teaches or suggests that the bus switch line is selectively switched in response to an event initiation. The Examiner cites Col. 5, lines 31-45 as teaching this limitation. At the cited reference, Shinohara merely teaches that a bus switch may be used as a switching means for switching between two buses. In contrast, Applicant's claim requires that *the bus switch line is selectively switched between the first device and the host in response to an event initiation*. Shinohara fails to teach or suggest an event initiation. Thus, not all of the limitations of Applicant's claims are shown in the cited reference. Thus, Claims 31-32 are believed allowable.

PAGE 11/13 * RCVD AT 8/10/2005 6:59:02 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/0 * DNIS:2738300 * CSID:4087208381 * DURATION (mm-ss):05-02

The Examiner's argument regarding Claim 32 is improper, and Applicant respectfully requests that it be withdrawn. The Examiner has rejected Claims 31-32 under 35 U.S.C. § 102(b). Thus a single reference is asserted as showing all of the limitations in the Claim. However, the Examiner refers to "Dent" in the explanation of the rejection. A combination of more than one reference is not proper for a § 102(b) rejection. Applicant respectfully requests that the Examiner either withdraw this improper rejection and allow Claims 31-32 to issue with Claims 1-30 and 33-40, or in the alternative, Applicant requests that the Examiner reissue a new non-final office action with a properly reformulated rejection.

However, regardless of the formulation of the Examiner's rejection, combining the teachings of Shinohara with Dent will not result in Applicant's invention. It is clear that Dent et al. teach a system where the host processor does not have direct access, i.e., is not connected, to memory components via a bus. All memory accesses are controlled by the DMA controller. Dent at al. do not teach that the control processor (host) is connected to one or more second devices, e.g., memory devices, via a signal line, or bus. Instead Dent et al. teach a system where the control processor (host) is connected to the DMA controller via a data and address bus. This is in contrast to Applicant's claimed invention. Thus, there is no motivation to combine the references, and doing so cannot result in Applicant's claimed invention.

PAGE 12/13 * RCVD AT 8/10/2005 6:59:02 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/0 * DNIS:2738300 * CSID:4087208381 * DURATION (mm-ss):05-02

09/888,105
Docket No.: 42P11839

CONCLUSION

In view of the foregoing, Claims 1-40 are all in condition for allowance. If the Examiner has any questions, the Examiner is invited to contact the undersigned at (703) 633-6845. Early issuance of Notice of Allowance is respectfully requested. Please charge any shortage of fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 02-2666 and please credit any excess fees to such account.

Respectfully submitted,

Dated: 10 Aug. 2005

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PAGE 13/13 * RCVD AT 8/10/2005 6:59:02 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/0 * DNIS:2738300 * CSID:4087208381 * DURATION (mm-ss):05-02